

Drafts Pending Active

- L1: (159631) gate.clm. or floating.clm.
- L2: (14651) 1 and ((non adj. volatile) or (floating adj. gate))
- L3: (677) 2 and (floating adj. gate).clm.
- L4: (3007) 3 and (oxide.clm.)
- L5: (1019) 4 and (sidewall\$1 or spacer\$1).clm.
- L6: (918) 5 and ((thermal adj. oxidation) or (oxide adj. layer))
- L7: (610) 5 and (thermal and oxidation)
- L8: (376) 7 and (barrier or diffusion)
- L9: (376) 8 and (spacer\$1.clm. or (side adj. wall\$1).clm. or sidewall\$1.clm)
- L10: (229) 9 and (buffer or (second near4 spacer\$1) or (second near5 sidewall\$1))
- L11: (180) 9 and (oxidation.clm. or thermal.clm. or RTO.clm.)
- L12: (66) 11 and (thermal adj. oxidation).clm.
- L13: (66) 11 and (thermal near oxidation).clm.
- L14: (63) 13 and (second near5 spacer\$1 or sidewall\$1 or (side adj. wall\$1))

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- (0) ("thinadjfilm/nearresistor").PN.
- (0) ("thinadjfilm/nearresistor").PN.
- (150130) thin adj film

#	IPR	P	Document ID	Issue Date	Page	Title	Current IP	Current XN	Retrival	Inventor	G	C	F	E	S
33	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6635532	20031021	18	Method for fabricating NOR type flash memory device having desired gate profile	438/259	257/E21.68		Song, Yun-Heub et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B2				438/257	257/E21.20							
34	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6620681	20030916	18	Semiconductor device	438/257	257/296		Kim, Min et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				438/257	257/300							
35	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6593187	20030715	20	Method to fabricate a square poly spacer in flash memory device with reduced film thickness	438/257	257/E21.68		Hsieh, Chia-Ta	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				438/257	257/E21.20							
36	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6589840	20030708	8	Nonvolatile memory device with reduced film thickness	438/257	438/596		Tseng, Horng-Huei	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B2				438/257	257/300							
37	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6569736	20030527	8	Method for fabricating square polysilicon spacer	438/267	438/596		Hsu, Cheng-Yuan et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				438/267	257/300							
38	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6509600	20030121	10	Flash memory cell	257/301	257/314		Lim, Min-Gyu	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B2				257/315	257/315							
39	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US RE37959	20030107	30	Semiconductor integrated circuit device	438/258	257/E21.20		Komori, Kazuhiro et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	E				438/258	257/314							
40	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6503785	20030107	17	Flash memory cell with contactless bit line	438/211	257/314		Chen, Chieh-Feng	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B2				438/211	257/315							
41	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6455888	20020924	18	Memory cell structure for elimination of crosstalk	257/315	257/E21.68		Early, Kathleen R. et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				257/315	257/E21.68							
42	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6355527	20020312	8	Method to increase coupling ratio of source	438/265	257/E21.68		Lin, Yai-Ken et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				438/265	257/E21.68							
43	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6323086	20011127	10	Flash memory structure using sidewall floating	438/257	257/E21.20		Hsu, Louis L. et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>	B1				438/257	257/314							
44	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	US 6323085	20011127	12	High coupling	438/257	257/E21.68		Sandhu, Sukesh et al.	<input checked="" type="checkbox"/>				
		<input checked="" type="checkbox"/>					438/257	257/315							

EAST - [resistor.wsp.]

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Document ID: Issue Date: Pages: Title: Current On Current X# Retrieval: Inventor: S C P F

71	P	F	C	US 2001051720	Flash memory structure using sidewall floating 257/315	257/E21.20	9.	Gambino, Jeffrey	P	C	F	F	F
75	P	F	C	US 6765259	Non-volatile memory using sidewall floating 257/315	257/316	9.	P. et al.	C	C	C	C	C
76	P	F	C	US 6756631	B2 transistor array implement 257/316	257/317	Wu, Ching-Yuan	P	C	F	F	F	
77	P	F	C	US 6746918	B2 stacked-gate cell structure and its NAND- 257/317	257/319	Wu, Ching-Yuan	P	C	F	F	F	
78	P	F	C	US 6744664	B2 Methods of fabricating a stack-gate non-volatile 438/257	257/314	Wu, Ching-Yuan	P	C	F	F	F	
79	P	F	C	US 6737344	B2 dual-bit floating-gate flash cell structure and 365/185.03	365/189.01	Wu, Ching-Yuan	P	C	F	F	F	
80	C	F	C	US 6710396	B1 Method for manufacturing nonvolatile 254/321	257/E21.20	Yamagata, Satoru et al.	P	C	F	F	F	
81	P	F	C	US 6706601	B1 self-aligned split-gate flash cell structure and 257/315	257/314	Wu, Ching-Yuan	P	C	F	F	F	
82	P	F	C	US 6703661	B1 Method of forming tiny silicon nitride spacer 438/266	257/321	LiU, Hung-Hsin et al.	P	C	F	F	F	
83	P	F	C	US 6699753	B2 contactless NOR-type memory array and its fabri- 257/315	257/314	Wu, Ching-Yuan	P	C	F	F	F	
84	P	F	C	US 6696329	B2 Method of manufacturing an array of non-volatile 438/201	257/315	Ma, Yueh Yale et al.	P	C	F	F	F	
85	P	F	C	US 6690058	B2 Method of manufacturing semiconductor device 438/211	257/316	Nakagawa, Shinichi	P	C	F	F	F	
					B2 self-aligned multi-bit	257/390	Wu, Ching-Yuan	P	C	F	F	F	